Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-27. (canceled)

28. (Previously presented) A method for controlling a non-volatile semiconductor memory system, the method comprising:

defining a plurality of physical blocks in a cell array of non-volatile semiconductor memory cells, each of the physical blocks including a plurality of non-volatile memory cells adapted for storing data;

storing address mapping information between the physical blocks and corresponding logical blocks in the physical blocks;

defining within the cell array at least first and second zones, each zone including at least one of the physical blocks;

preparing, in response to a power supply being turned on, a prepared address translation table comprising address translation information between logical blocks and physical blocks within the memory array, the prepared address translation table including address translation information for logical block addresses within at least the first zone and not including address translation information for logical block addresses within at least the second zone; and

determining that a requested logical block is not within the prepared address translation table and subsequently preparing a second address translation table comprising address translation information for logical block addresses within the second zone.

29. (Previously presented) A method for controlling a non-volatile semiconductor memory system, as set forth in claim 28, the method further comprising selectively replacing a defective physical block including defective cells with a redundant physical block so that, for each area, a quantity of defective physical blocks is less than or equal to a predetermined number.

30. (Previously presented) A method for controlling a non-volatile semiconductor memory system, the method comprising:

dividing a cell array of non-volatile semiconductor memory cells into a plurality of physical blocks;

storing in each of the physical blocks information corresponding to each relationship between the physical blocks and corresponding ones of logical blocks managed by the system;

storing in a random access memory in the system a first table for managing corresponding relationships between a first set of the logical blocks and the physical blocks of a first physical block zone including one or more of the physical blocks; and

determining in response to an access from a host that a requested logical block is not within the first table and subsequently storing in the random access memory a second table comprising relationships between a second set of the logical blocks and the physical blocks of a second physical block zone including one or more of the physical blocks.

31. (Previously presented) A method for controlling a non-volatile semiconductor memory system, as set forth in claim 30, the method further comprising selectively replacing a defective physical block including defective cells with a redundant physical block so that, for each area, a quantity of defective physical blocks is less than or equal to a predetermined number.

32. (New) A method for controlling a memory system including a non-volatile semiconductor memory, the method comprising:

providing a translation table mapping logical block addresses to physical block area addresses within a non-volatile semiconductor memory, each physical block area address identifying a physical block area within the non-volatile semiconductor memory having more than one physical block within the physical block area,

wherein the physical block of the non-volatile memory has a data storage capacity equal to or larger than a storage capacity of a logical block; and

seeking a physical block by converting a requested logical block address to a physical block area address according to the translation table and then determining which physical block within the physical block area corresponds to the requested logical block address.

33. (New) The method of claim 32, wherein the logical block addresses are defined external to the memory system and wherein the seeking includes searching for physical blocks within the physical block area.

34. (New) The method of claim 32, wherein the memory system is adapted to generate the translation table in response to applying operating power to the memory system by searching the non-volatile memory.

35. (New) The method of claim 34, wherein the translation table is stored in a random access memory (RAM) within the memory system.

36. (New) The method of claim 32, further comprising checking a physical format of a non-volatile memory to determine if the physical format is supported by the memory system before the translation table is generated as part of a power up routine.

37. (New) The method of claim 32, wherein each physical block area consists of two physical blocks.

38. (New) A method for controlling a non-volatile semiconductor memory system which comprises the steps of:

dividing a cell array of non-volatile memory cells into a plurality of physical blocks;

storing mapping information between the physical blocks and corresponding logical blocks in a storage region of each of the physical blocks, wherein the logical blocks are managed by the system;

defining an area formed by more than one of the physical blocks; and

forming a table for managing address relationships between the logical blocks and the physical blocks of non-volatile memory cells, the table stored in a random access memory of the memory system, the table formed by searching the storage regions of physical blocks,

wherein the table includes at least one logical block address entry that maps to an address within the cell array corresponding to two or more physical blocks and wherein the storage

regions of the two or more physical blocks include two or more corresponding logical block addresses and one of the corresponding logical block addresses is the logical block address of the at least one logical block address entry.

39. (New) The method of claim 38, wherein the physical blocks have a storage capacity at least as large as the logical blocks.

40. (New) The method of claim 38, further comprising seeking a physical block by converting a requested logical block address to a physical block area address according to the table and then searching for a physical block within the physical block area that corresponds to the requested logical block address.